

**L-Band Avionics Transistor**

The high power pulsed avionics transistor part number IB1012S50 is designed for L-Band avionics systems operating at 1025 to 1150 MHz. While operating in class C mode under DME pulse conditions at  $V_{CC}=50V$ , this common base device supplies a minimum of 50 watts of peak pulse power. It utilizes a low loss internal input impedance matching structure to yield maximum device gain and to ease the implementation of external matching circuitry. The new generation bipolar transistor geometry utilizes a gold metallization system to achieve maximum reliability. Emitter ballast resistance is incorporated on the active cell for optimum thermal distribution and maximum reliability. All devices are 100% screened for large signal RF parameters.



**Silicon Bipolar**

- Ultra-high  $f_T$

**Class C Operation**

- High Efficiency

**Common Base Configuration**

- Single Power Supply

**Gold Metal**

- Maximum Reliability

**Emitter Ballasting**

- Optimum Thermal Distribution

**Internal Impedance Matching**

- Ease of Use
- Ultra-low Loss Design

**Be0 Package**

- Unmatched Thermal Reliability

**RF Test Fixture**

- Broadband
- Matched to 50 $\Omega$
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning Allowed
- Micro-strip structure on soft pc board with dielectric constant 10.2

*TYPICAL DATA      TYPICAL DATA      TYPICAL DATA      TYPICAL DATA*

General Information	Test Sequence	Freq	PIN	RL	POUT	GP	dG	IC	nc	Droop	VSWR-S	VSWR-LMT
IB1012S50	Name	(MHz)	(W)	(dB)	(W)	(dB)	(dB)	(A)	(%)	(dB)	1.5:1	3:1
Date: 4/2/2009												
Asbly Lot - SN: D4090-10	Nominal	1025	5.0	-12.0	56.3	10.52		2.400	46.9	0.06	S	P
Wafer: GL1E-2-1												
Test Fixture: 2397	Nominal	1090	5.0	-18.0	59.0	10.72	0.20	2.200	53.6	0.07	S	P
Pass / Fail: Device Passes												
OPERATOR: FB	Nominal	1150	5.0	-18.0	58.0	10.64		2.400	48.3	0.07	S	P
Vcc=50V Pulse:10us-1%												

**MAXIMUM RATINGS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Collector-Emitter Voltage	$V_{CES}$	--	85	V	--
BD	Emitter-Base Voltage	$V_{EBO}$	--	2	V	--
BD	Storage Temperature Range	$T_{STG}$	-55	+150	°C	--
BD	Operating Junction Temperature Range	$T_J$	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

**THERMAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	TBD	°C/W	$V_{CC}=50V$ , Pulse format= DME (10 $\mu$ s, 1%), $T_F=25\pm 5^\circ C$ , $P_{IN}=5W$ , $N_C=45\%$
Note	Screen 'BD' = parameter qualified By Design.					

**PROCESSING SPECIFICATIONS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

**DC ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Collector-Emitter Breakdown Voltage	$BV_{CES}$	85	--	V	$I_C = 10mA$ , $V_{BE} = 0V$ , $T_F = 25\pm 5^\circ C$ .
100%	Zero Base Voltage Collector Leakage Current	$I_{CES}$	--	0.1	mA	$V_{CE} = 50V$ , $V_{BE} = 0V$ , $T_F = 25\pm 5^\circ C$ .
100%	DC Current Gain	$H_{FE}$	10	100	--	$V_{CE} = 5V$ , $I_C = 0.1A$ , $T_F = 25\pm 5^\circ C$ .

**RF ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	RL	18	-10	dB	$V_{CC}=50V$ , $P_{IN}=5W$ , Pulse = Note 2, $T_F=25\pm5^\circ C$ , $F=F1$ .
BD	Maximum Overdrive	$P_{IN(MAX)}$	--	6.7	W	$V_{CC}=50V$ , Pulse = Note 2, $T_F=25\pm5^\circ C$ , $F=F1$ .
100%	Power Gain	$G_P$	10.0	11.5	dB	$V_{CC}=50V$ , $P_{IN}=5W$ , Pulse = Note 2, $T_F=25\pm5^\circ C$ , $F=F1$
100%	Output Power	$P_{out}$	50.0	70.6	dB	$V_{CC}=50V$ , $P_{IN}=5W$ , Pulse = Note 2, $T_F=25\pm5^\circ C$ , $F=F1$
100%	Collector Efficiency ( $P_o/I_c/V_{CC}$ )	$N_c$	45	75	%	$V_{CC}=50V$ , $P_{IN}=5W$ , Pulse = Note 2, $T_F=25\pm5^\circ C$ , $F=F1$ .
100%	Pulse Amplitude Droop	Droop	-0.5	0.5	dB	$V_{CC}=50V$ , $P_{IN}=5W$ , Pulse = Note 2, $T_F=25\pm5^\circ C$ , $F=F1$ .
100%	Stability into 1.5:1 VSWR	VSWR-S	--	--	--	$V_{CC}=50V$ , $P_{IN}=5W$ , Pulse = Note 2, $T_F=25\pm5^\circ C$ , $F=F1$ . Rotate 1.5:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse.
100%	Load Mismatch Tolerance	VSWR-LMT	3:1	--	--	$V_{CC}=50V$ , $P_{IN}=5W$ , Pulse = Note 2, $T_F=25\pm5^\circ C$ , $F=F1$ . Rotate 3:1 output VSWR through 360° phase. Survival.
BD	Pulse Risetime	RT	--	80	ns	$V_{CC}=50V$ , $P_{IN}=5W$ , Pulse = Note 2, $T_F=25\pm5^\circ C$ , $F=F1$ . Measure between 10% and 90% detected power points.
Note 1	F1 = 1025/1090/1150 MHz.					
Note 2	Pulse format = DME (10µs, 1%)					
Note 3	$T_F$ = Device flange temperature.					
Note 4	Screen 'BD' = parameter qualified By Design.					

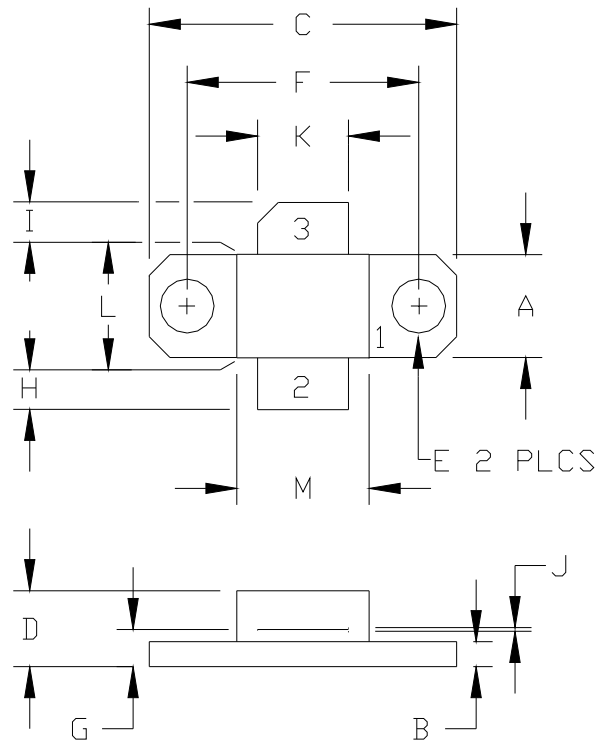
**RF TEST FIXTURE IMPEDANCE CHARACTERISTICS**

Frequency (MHz)	$Z_{IF}$ ( $\Omega$ )	$Z_{OF}$ ( $\Omega$ )
1025	4.53 -j4.03	12.64 +j3.25
1090	3.98 -j3.06	17.20 +j2.23
1150	3.75 -j2.30	21.62 -j2.69

Impedance Definition		
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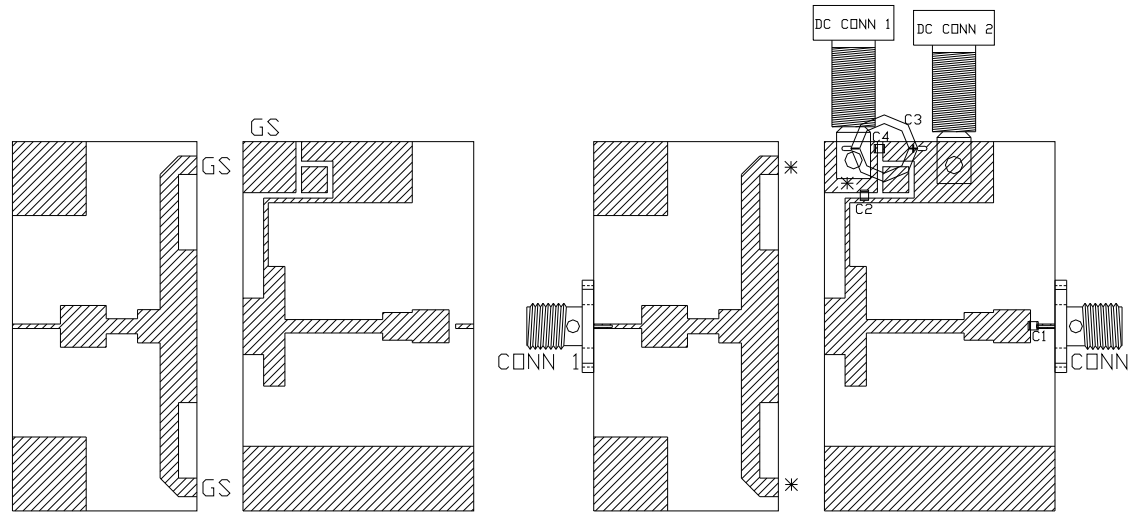
**PACKAGE DIMENSIONAL OUTLINE DRAWING**



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.243	0.253	6.17	6.43
B	0.055	0.065	1.40	1.65
C	0.739	0.749	18.77	19.02
D	0.178	0.188	4.52	4.78
E	0.125	0.135	3.18	3.43
F	0.555	0.565	14.10	14.35
G	0.082	0.092	2.08	2.34
H	0.080	0.150	2.79	3.56
I	0.080	0.150	2.03	2.54
J	0.004	0.006	0.10	0.15
K	0.215	0.225	5.46	5.72
L	0.245	0.255	6.22	6.48
M	0.315	0.325	8.00	8.26

PIN SCHEDULE	
1	BASE
2	EMITTER
3	COLLECTOR

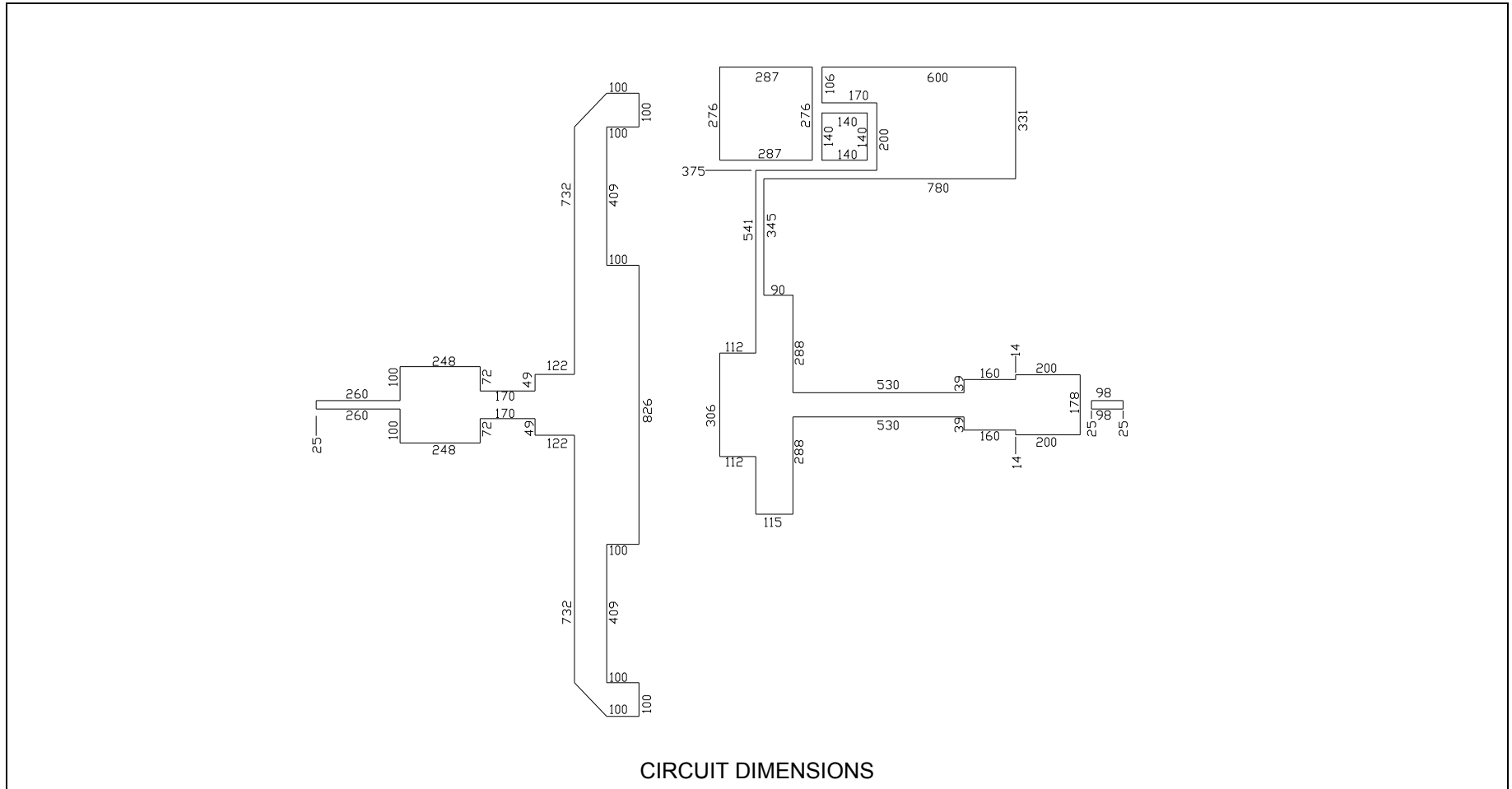
**RF TEST FIXTURE**

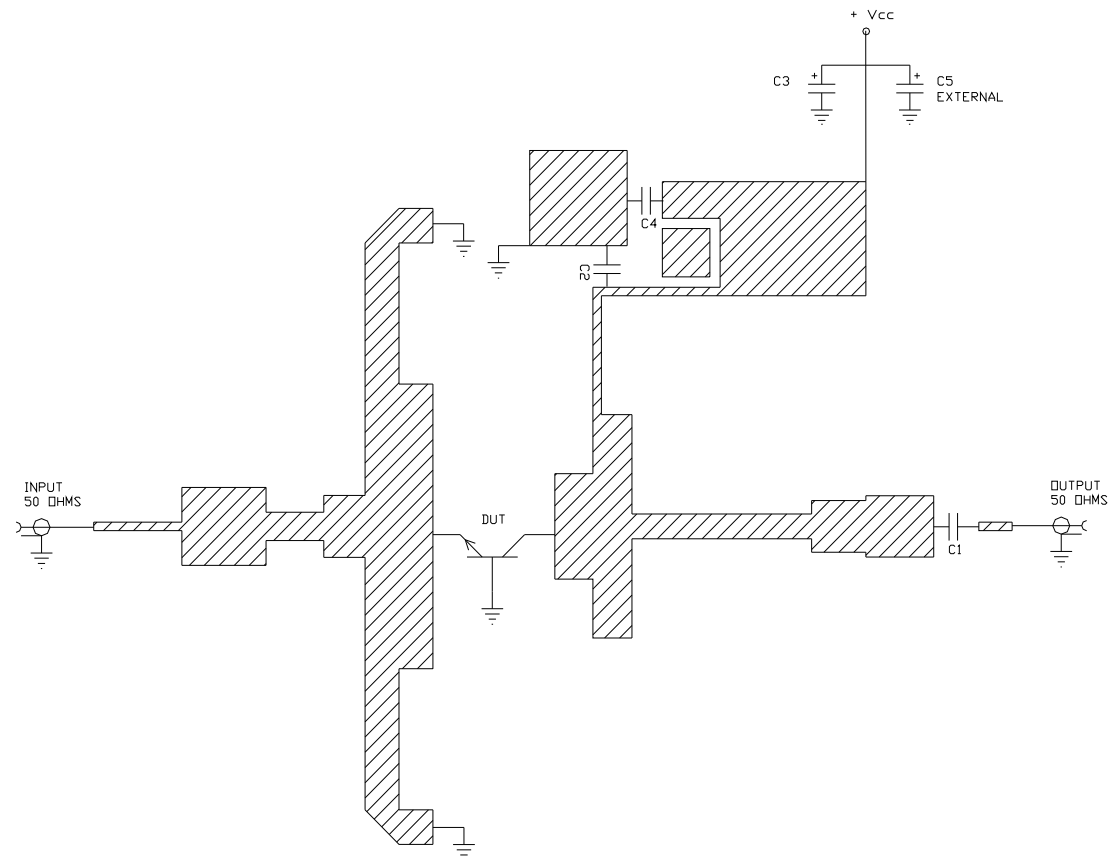


COMPONENT	DESCRIPTION
DUT	TRANSISTOR #IB1012S50, MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS #RD 3010 .025" 1oz. Cu
C1, C2	CHIP CAPACITOR ATC100A-100 pF
C3	ELECTROLYTIC CAPACITOR, 68uF / 63V
C4	TANTALUM AVX 4.7uF 50V low ESR=0.3ohms
C5 (NOT SHOWN)	ELECTROLYTIC CAPACITOR 4700uF, 50V
GS (3 PLACES)	GROUND SHIM, COPPER, TH=0.001"
CONN 1, CONN 2	SMA CONNECTOR, DS #2052-5636-02
INPUT PC BOARD CARRIER	2 INCH BRASS-03 (1")
OUTPUT PC BOARD CARRIER	2 INCH BRASS-04 (1.25")
TRANSISTOR CARRIER	2 INCH COPPER-01 (P32)
TRANSISTOR CLAMP	NORYL CLAMP-01 (P32)
ALUMINUM HEATSINK	2 INCH HEAT SINK-11
DC CONN 1	BANANA JACK, BLACK
DC CONN 2	BANANA JACK, RED
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

**ASSEMBLY AND PARTS LIST**

**RF TEST FIXTURE**





ELECTRICAL SCHEMATIC

**DEFINITIONS**

<b>Data Sheet Status</b>	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
<b>Maximum Ratings</b>	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

**WARNING**

<b>Product and environmental safety - toxic materials</b>
This product contains beryllium oxide. The product is entirely safe provided that the BeO base is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with general or domestic waste.

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