Part Number: ILD3135M120

Integra
TECHNOLOGIES, INC.

S-Band Radar Transistor

Part number ILD3135M120 is designed for S-Band radar applications operating over the 3.1 – 3.5 GHz instantaneous frequency band. Under 300us / 10% pulsing conditions it supplies a minimum of 120 watts of peak output power with 10dB gain typically. Specified operation is with Class AB bias. The broadband test fixture includes a temperature compensated bias network. All devices are 100% screened for large signal RF parameters in a fixed tuned broadband matching circuit / test fixture. The use of external tuners is not allowed during screening. This device is rated for a peak output power level of P_{PEAK} = 120W @ 10% duty factor. This corresponds to an average power P_{AVG} = 12W.

Silicon LDMOS FET
- High Power Gain
- Excellent thermal stability
- Gold Metal

Gold Metal System
- Complete Gold System
- LDMOS with Gold Metal
- Gold Bond Wires
- Gold Package Metal
- Maximum Reliability

Class AB Operation
- Specified with AB bias

Internal Impedance Matching
- Ease of Use
- Ultra Low Loss Design

BeO Free Package
- Metal Based
- Epoxy Seal

High Power RF Test / Fixture
- Broadband
- Matched to 50 Ω (ohms)
- Temperature Compensated Bias
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

TYPICAL DATA TYPICAL DATA TYPICAL DATA TYPICAL DATA

FREQ (GHz)	PW (us)	Duty (%)	V_{DD} (V)	I_{DQ} (mA)	P_{IN} (W)	IRL (dB)	P_{OUT} (W)	G_P (dB)	I_D (A)	N_D (%)	Droop (dB)	VSWR-S 3:1
3.1	300	10	32	50	14	-18	161	10.6	12.13	42	-0.20	Pass
3.3	300	10	32	50	14	-10	160	10.5	12.16	41	-0.20	Pass
3.5	300	10	32	50	14	-14	141	10.0	10.70	41	-0.10	Pass

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MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	65	V	--
BD	Gate-Source Voltage	V_{GS}	-0.5	12	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
BD	CW Operation	--	--	--	--	Not rated for CW operation.
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.17	°C/W	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=25±5°C, P_{OUT}=120W, N_D=38%
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	BV_{DSS}	65	--	V	I_{DS}=10mA, V_{GS}=0V, T_F=25±5°C
100%	Drain Leakage Current	I_{DSS}	--	10	uA	V_{DS}=32V, V_{GS}=0V, T_F=25±5°C
100%	Operating Gate Voltage	V_{GS}	2.5	4.0	V	V_{DS}=5V, I_D=0.1A, T_F=25±5°C
100%	Gate Leakage Current	I_{GSS}	--	1.0	uA	V_{GS}=5V, V_{DS}=0V, T_F=25±5°C

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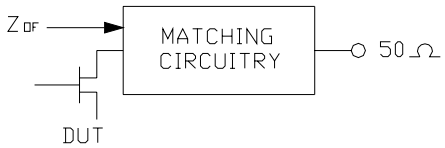
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	-18	-7	dB	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.
100%	Output Power	P_O	120	200	W	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.
100%	Drain Efficiency	N_D	35	50	%	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1.
100%	Drain Efficiency	N_D	35	50	%	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F2.
100%	Drain Efficiency	N_D	35	50	%	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F3.
100%	Drain Current	I_D	9.0	14.0	A	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.
100%	Pulse Amplitude Droop	D	-0.5	+0.5	dB	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.
100%	Insertion Phase	IP	-30	+30	DEG	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F3.
100%	3:1 Load Mismatch Stability	VSWR-S	--	--	--	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3. Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least –65 dBc.
Note 1	All devices are marked with delta insertion phase offsets from -1 thru -12 indicating 5° variations between -30° to +30° from reference.					
Note 2	V1 = 32V; I_{DQ1} = 40mA; PW1 = 300us; DF1 = 10%, P_{IN1} = 14W.					
Note 3	Test Frequencies: F1 = 3.1 GHz, F2 = 3.3 GHz, F3 = 3.5 GHz.					
Note 4	T_{F1} = 25±5°C = Device flange temperature.					
Note 5	Screen 'BD' = parameter qualified By Design.					

RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (GHz)	Z_{IF} (Ω)	Z_{OF} (Ω)
3.10	2.5 – j5.3	2.7 – j3.9
3.30	2.4 – j4.6	2.2 – j3.1
3.50	2.3 – j3.5	2.4 – j1.6
Impedance Definition		

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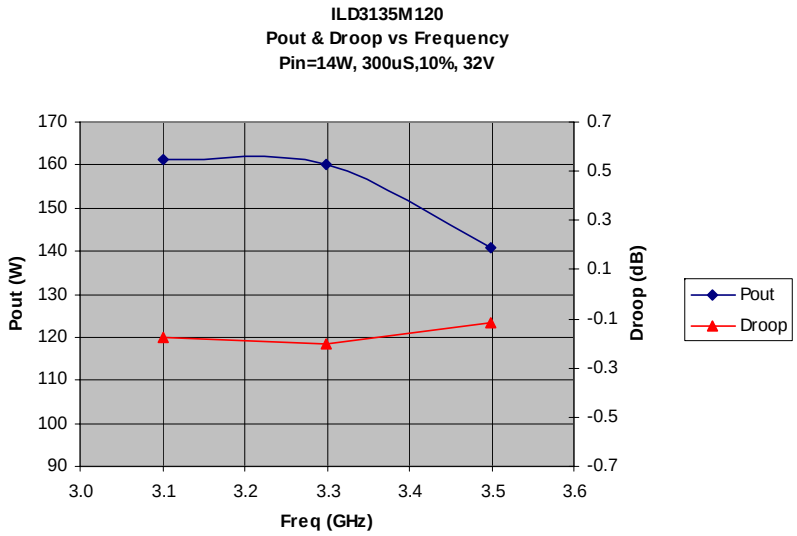
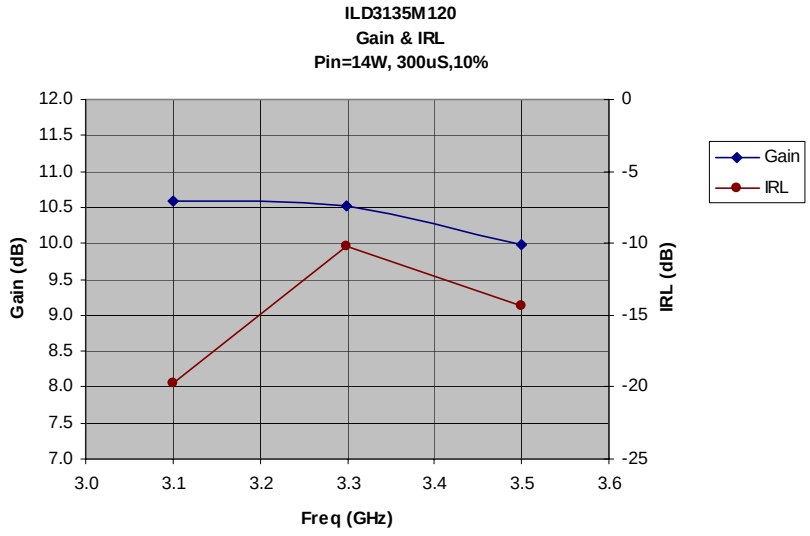
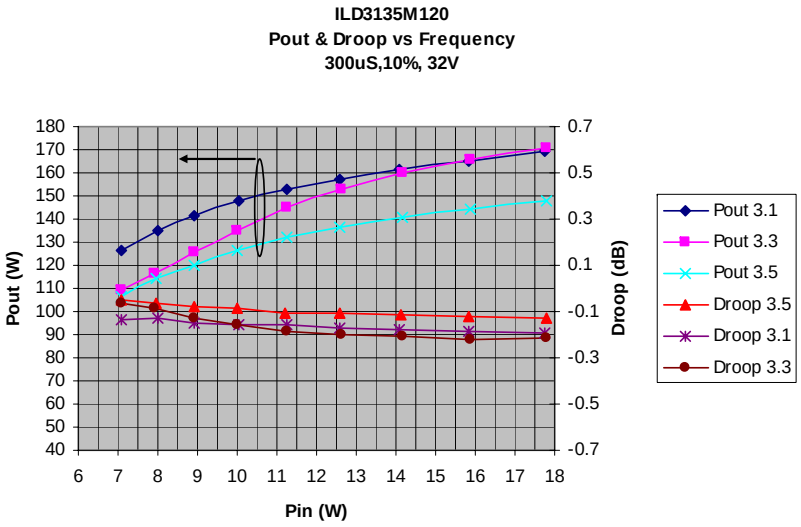
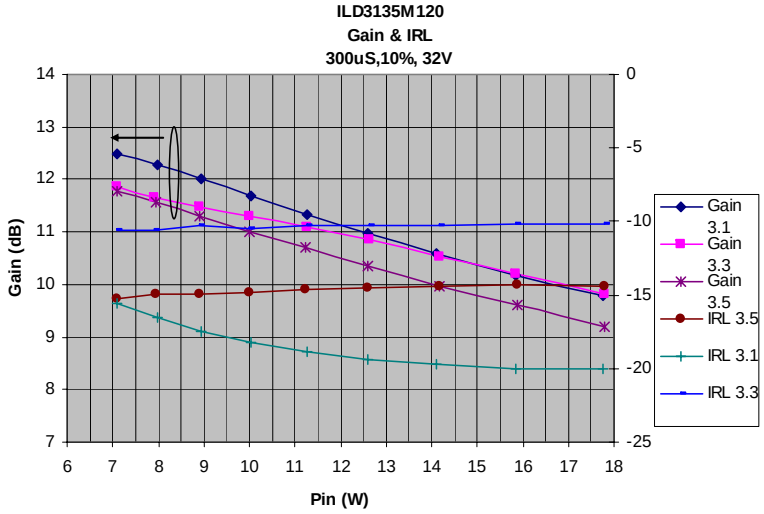
PERFORMANCE GRAPHS









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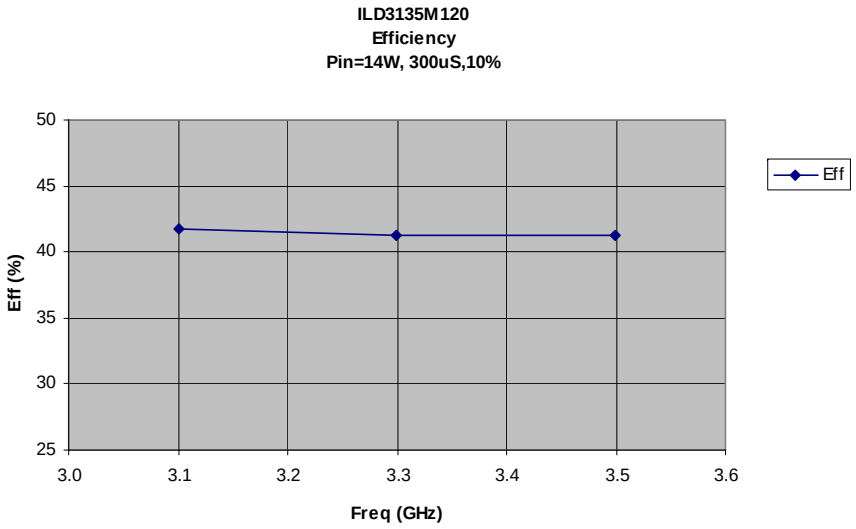

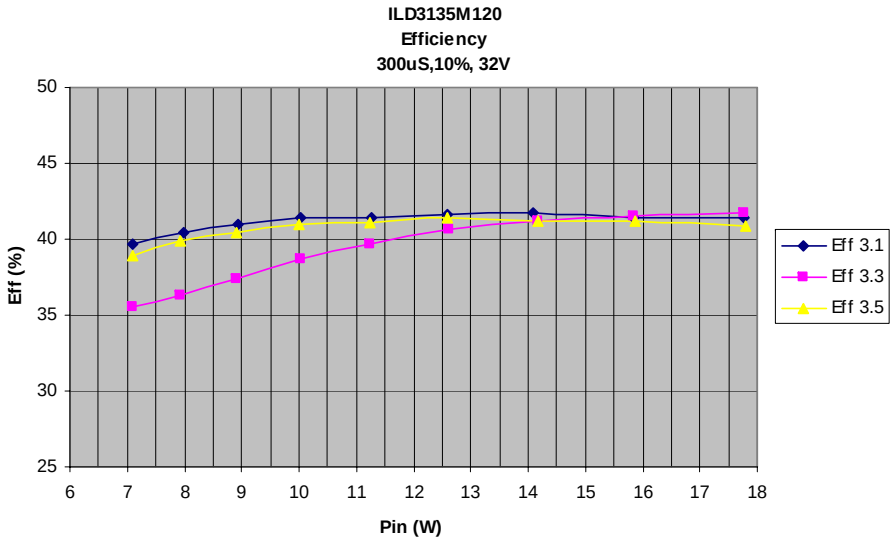

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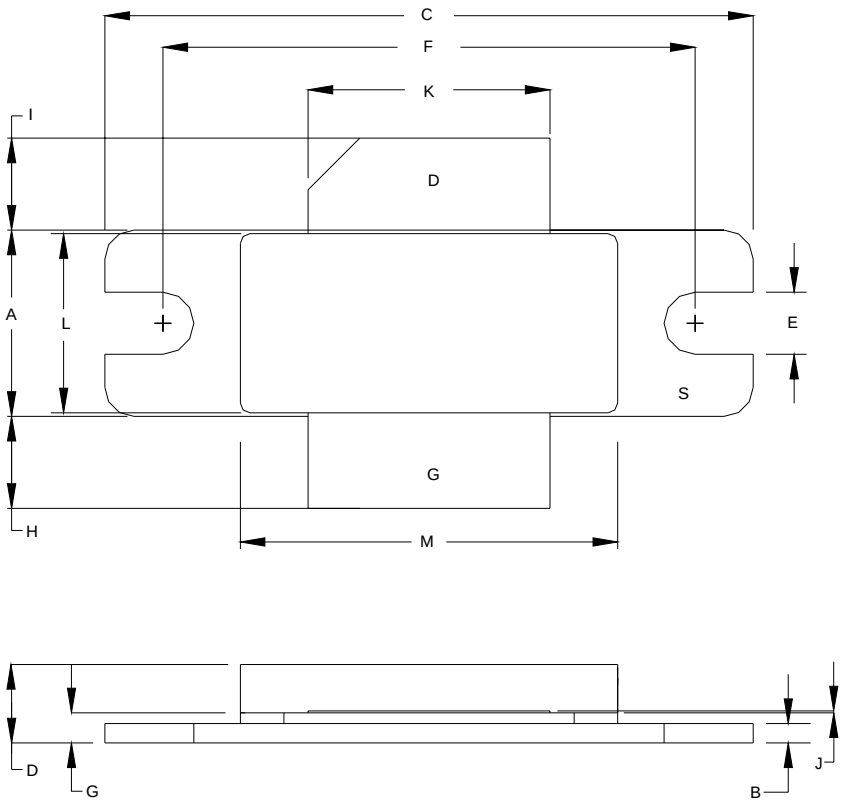
PACKAGE DIMENSIONAL OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.380	0.390	9.65	9.91
B	0.035	0.045	0.89	1.14
C	1.335	1.345	33.90	34.16
D	0.139	0.164	3.53	4.22
E	0.123	0.133	3.12	3.38
F	1.095	1.105	27.81	28.07
G	0.057	0.067	1.45	1.70
H	0.170	0.210	4.32	5.33
I	0.170	0.210	4.32	5.33
J	0.003	0.006	0.08	0.15
K	0.495	0.505	12.57	12.83
L	0.364	0.374	9.24	9.49
M	0.775	0.785	19.68	19.94

PIN SCHEDULE	
D	DRAIN
S	SOURCE
G	GATE

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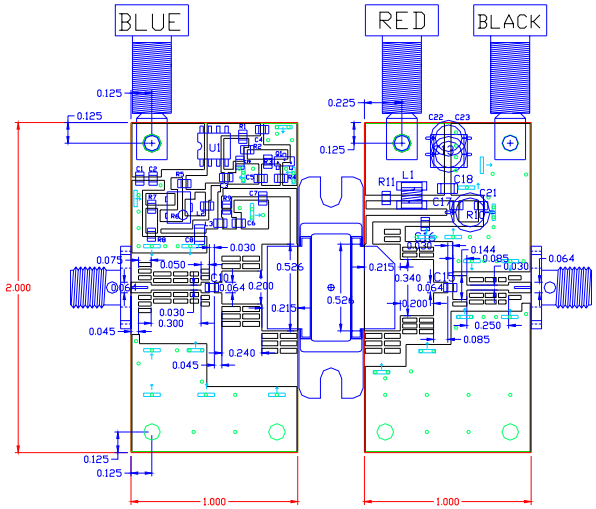
RF TEST FIXTURE – ASSEMBLY AND PARTS LIST



COMPONENT	DESCRIPTION
DUT	TRANSISTOR #ILD3135M120 MOUNT HARD TO THE RIGHT
PC BOARD	ROGER #RO4350B-03011, 30mil 1/1oz Copper
C1, C4, C6, C17	CAPACITOR 0.1UF , 0805 , 50V
C2, C3, C5, C9	CAPCITOR 39pF , ATC600F390J
C7, C10, C15, C16	CAPCITOR 39pF , ATC600F390J EDGE MNT
C8, C18	CAPACITOR 1uF , 1206 , 100V
C13	CAPACITOR 10uF, 2220, 50V , X7R
C14, C19	CAPACITOR 1uF, 0805, 25V
C20	ALUMINUM ELECTROLYTIC 4700uF , 50V
C21	CAP, 47uF, 50V, ELECTROLYTIC CAP
C22	CAP, 100uF, 50V, ELECTROLYTIC CAP
C23	CAP, 150uF, 50V, ELECTROLYTIC CAP
L1	IND , 5V5,1508
L2, L3	IND , FB , 120 OHM, 0805, 5A
U1	IC , VREG-ADJ,SOIC-8,LM317LM-ND
Q1	PMBT2222
R1	RESISTOR, 1K, 0805
R2, R3	RESISTOR, 3.9K 0805
R4	RESISTOR , 2.2K, 0805
R5	RESISTOR, 511, 0805
R8	RESISTOR, 150OHMS, 0805
R7, R9, R10, R11	RESISTOR, 5R1, 0805
R6	RESISTOR , VAR, 200, 4MM, 3224V, BURNS
GS-GS23	GROUND STRAP, FOLD AS SHOWN GS CAN BE USED INSTEAD OF PLATED VIAS
GS (PLATED THRU VIAS)	GROUND SHIM, COPPER TH=0.001
CONN 1, CONN 2	SMA CONNECTOR, DS #2052-5636-02
INPUT PCB CARRIER	2 INCH BRASS -3 (1")
OUTPUT PCB CARRIER	2 INCH BRASS -3 (1")
TRANSISTOR CARRIER	2 INCH COPPER -22
TRANSISTOR CLAMP	NORYL CLAMP -08
ALUMINUM HEAT SINK	2 INCH HEAT SINK -11
DC CONN 1	BANANA JACK, RED
DC CONN 2	BANANA JACK, BLACK
DC CONN 3	BANANA JACK, BLUE
DUT	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

TOLERANCES UNLESS NOTED			
.X ± .1	X° ± 1°	Integra TECHNOLOGIES, INC.	
.XX ± .02	X°X' ± 0°30'		
.XXX ± .005		ILD3135M120 RF TEST FIXTURE	
.XXXX ± .0002	FRACTION ±1/32		
MATERIAL: NOTED			
DRAWN: W. VEITSCHEGGER			
CHECKED: J. BURGER	SIZE A	DWG NO. ILD3135M120 RF TEST FIXTURE	REV D
APPROVED: J DAVIS	SCALE: 1:1	SHEET: 1 of 2	

CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSIONS

L:\Public\Controlled Documents\Controlled Drawings\RF Test Fixture Drawings\ILD3135M120 RF TEST FIXTURE_REV D.dwg

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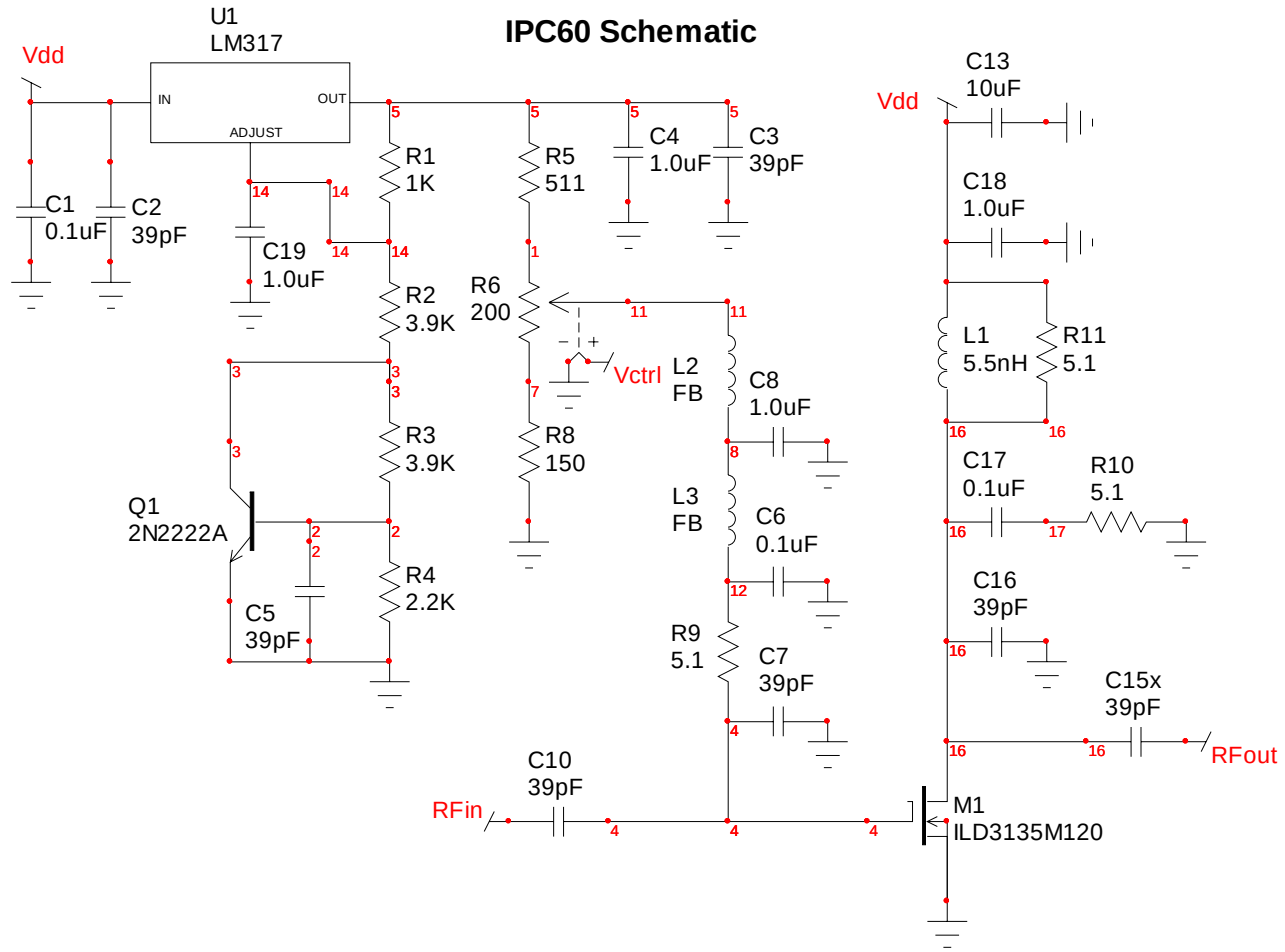
RF TEST FIXTURE – ELECTRICAL SCHEMATIC



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DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.

Maximum Ratings
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.

DISCLAIMER

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