## S-Band Radar Transistor - GaN

- GaN on SiC HEMT Technology
- $P_{OUT-PK}$ ≥ 115W @ 3ms/30%/46V
- 3.1-3.5GHz Instantaneous Operating Frequency Range
- Input and Output Internal Impedance Pre-matched Device
- Depletion Mode Device
- Negative Gate Voltage and Bias Sequencing Required
- Specified For Use Under Class AB Operation
- Metal Based Package Sealed With Ceramic-Epoxy Lid
- Gold Metallization System: Chip - Wire Bond - Package
- Package Size: W=0.800″ (20.32mm), L=0.400″ (10.16mm)
- 100% High Power RF Tested in Broadband RF Test Fixture


| PARAMETER | SYM | MIN | TYP | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| **DC ELECTRICAL SPECIFICATIONS** | | | | | | |
| Drain Leakage Current | $I_{D-OFF}$ | -- | 1.0 | -- | mA | $V_{DS}$=46V, $V_{GS}$=-6V, $T_{F1}$, S1 |
| Gate Threshold Voltage | $V_{GS-TH}$ | -- | -2.5 | -- | V | $V_{DS}$=46V, $I_D$=25mA, $T_{F1}$, S1 |
| | | | | | | |
| **RF ELECTRICAL SPECIFICATIONS** | | | | | | |
| Input Return Loss | IRL | -18 | -12 | -7 | dB | PIN1, V1, $I_{DQ1}$, PW1, DF1, F1, F2, F3, $T_{F1}$, S1 |
| Output Power | Po | 115 | -- | -- | W | PIN1, V1, $I_{DQ1}$, PW1, DF1, F1, F2, F3, $T_{F1}$, S1 |
| Drain Efficiency | $N_D$ | -- | 51 | -- | % | PIN1, V1, $I_{DQ1}$, PW1, DF1, F1, F2, F3, $T_{F1}$, S1 |
| Pulse Amplitude Droop | D | -0.50 | -0.20 | +0.30 | dB | PIN1, V1, $I_{DQ1}$, PW1, DF1, F1, F2, F3, $T_{F1}$, S1 |
| Delta Inter-pulse Insertion Phase | DIP | -30 | -- | +30 | DEG | PIN1, V1, $I_{DQ1}$, PW1, DF1, F1, F2, F3, $T_{F1}$, S1 |
| Load Mismatch Stability | VSWR-S | 2:1 | -- | -- | -- | PO=115W, V1, $I_{DQ1}$, PW1, DF1, F1, F2, F3, $T_{F1}$, S1 |
| Load Mismatch Tolerance | LMT | 3:1 | -- | -- | -- | PO=115W, V1, $I_{DQ1}$, PW1, DF1, F1, F2, F3, $T_{F1}$, S1 |
| **DC & RF TEST CONDITIONS** | | | | | | |
| Input Power 1 | PIN1 | 4.3 | 5.0 | 5.9 | W | -- |
| Drain Supply Voltage 1 | V1 | -- | | 46.0 | V | -- |
| Quiescent Drain Current 1 | $I_{DQ1}$ | -- | 25 | -- | mA | See Bias Sequencing Section |
| Pulse Width 1 | PW1 | -- | | 3 | ms | -- |
| Duty Factor 1 | DF1 | -- | | 30 | % | -- |
| Frequency 1 | F1 | -- | 3.1 | -- | GHz | -- |
| Frequency 2 | F2 | -- | 3.3 | -- | GHz | -- |
| Frequency 3 | F3 | -- | 3.5 | -- | GHz | -- |
| Flange Temperature 1 | $T_{F1}$ | 25 | 30 | 35 | °C | -- |
| Screening Level 1 | S1 | 100 | -- | -- | % | -- |



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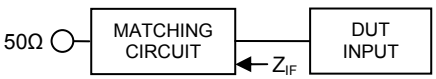
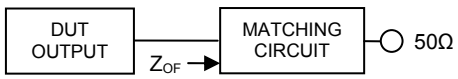
| PARAMETER | SYM | MIN | MAX | UNITS | SCREEN | CONDITIONS |
|---|---|---|---|---|---|---|
| **MAXIMUM RATINGS** | | | | | | |
| Drain-Source Voltage | $V_{DS}$ | -- | 60 | V | BD | $T_F$ = 25°C |
| Gate-Source Voltage | $V_{GS}$ | -10 | 0 | V | BD | $T_F$ = 25°C |
| Storage Temperature Range | $T_{STG}$ | -55 | +150 | °C | BD | -- |
| Operating Junction Temperature | $T_J$ | -55 | +200 | °C | BD | -- |
| | | | | | | |
| **PROCESS SPECIFICATIONS** | | | | | | |
| DC Wafer Probe | -- | -- | -- | -- | 100% | Per Integra Spec |
| Wafer DC, RF Qualification | -- | -- | -- | -- | Q1 | Per Integra Spec |
| Wire Bond Strength | -- | -- | -- | -- | LM | Per Integra Spec |
| Pre-cap Visual Inspection | -- | -- | -- | -- | 100% | Per Integra Spec |
| Gross Leak Test – MIL-STD-750D | -- | -- | -- | -- | 100% | Method 1071.6 C |
| | | | | | | |
| **THERMAL RESISTANCE** | | | | | | |
| Peak Thermal Resistance Per Rated RF Specification | $R_{TH(JC)}$ | -- | 0.36 | °C/W | BD | $T_F$=25°C, Pd=156W pK |
| | | | | | | |
| **SCREENING LEVELS** | | | | | | |
| Parameter Qualified By Design | BD | -- | -- | -- | -- | -- |
| Parameter Qualified By 3 Pieces (min) Per Wafer | Q1 | -- | -- | -- | -- | -- |
| Parameter Qualified By Assembly Line Monitor | LM | -- | -- | -- | -- | -- |

**RF TEST FIXTURE – BROADBAND**

► Broadband RF Test Fixture. Provides Device Impedance Matching to 50Ω Across the Rated Operating Frequency Range.

► Electronic CAD Drawing File Available Upon Request. Includes Circuit Dimensions and Parts List.

► Reference Design PCB: Rogers RO4350B-03011, DK=3.48.

| FREQUENCY (GHz) | $Z_{IF}$(Ω) | $Z_{OF}$(Ω) |
|---|---|---|
| 3.1 | 4.9 – j5.9 | 7.2 – j4.3 |
| 3.3 | 4.2 – j4.8 | 6.8 – j3.5 |
| 3.5 | 3.8 – j3.6 | 6.4 – j2.5 |
| Impedance Definition<br>(50 ohm launcher 183 mils wide) |  |  |

**DC BIAS SEQUENCING**

| Turn ON GaN Device | Turn OFF GaN Device |
|---|---|
| 1. RF Power OFF<br>2. Set VGS = -5V (Negative Voltage to pinch off)<br>3. Measure VDS impedance, should be pinched off.<br>4. Turn ON VDD voltage.<br>5. Slowly increase VGS until bias current IDQ is set.<br>6. Turn ON RF Power | 1. Turn OFF RF Power<br>2. Turn OFF VDD voltage<br>3. After VDD is discharged, set VGS = -5V<br>4. Turn OFF VGS voltage. |



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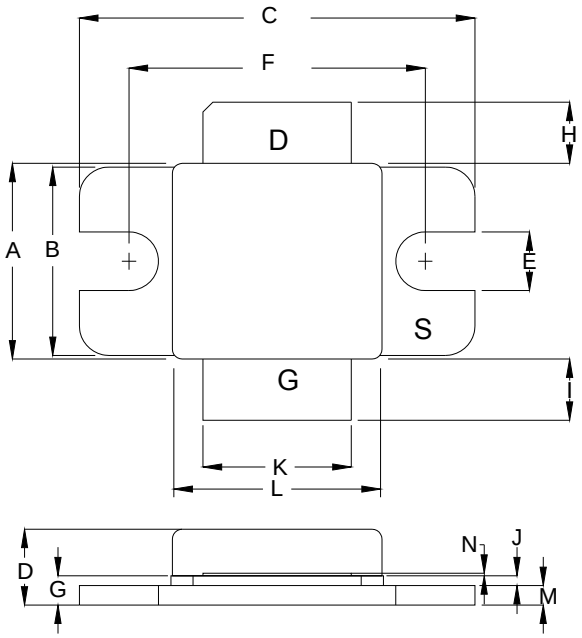
## PACKAGE OUTLINE DRAWING




| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.395 | 0.405 | 10.03 | 10.29 |
| B | 0.380 | 0.390 | 9.65 | 9.91 |
| C | 0.795 | 0.805 | 20.19 | 20.45 |
| D | 0.143 | 0.177 | 3.63 | 4.49 |
| E | 0.115 | 0.125 | 2.92 | 3.17 |
| F | 0.595 | 0.605 | 15.11 | 15.37 |
| G | 0.053 | 0.065 | 1.35 | 1.65 |
| H | 0.110 | 0.140 | 0.28 | 0.36 |
| I | 0.110 | 0.140 | 0.28 | 0.36 |
| J | 0.018 | 0.022 | 0.046 | 0.056 |
| K | 0.295 | 0.305 | 7.49 | 7.74 |
| L | 0.425 | 0.435 | 10.80 | 11.05 |
| M | 0.035 | 0.045 | 0.89 | 1.14 |
| N | 0.004 | 0.007 | 0.10 | 0.17 |

| PIN SCHEDULE | |
|---|---|
| D | DRAIN |
| S | SOURCE |
| G | GATE |



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| DEFINITIONS | |
|---|---|
| **DATA SHEET STATUS** | |
| Proposed Specification | This data sheet contains proposed specifications. |
| Preliminary Specification | This data sheet contains specifications based on preliminary measurements and data. |
| Product Specification | This data sheet contains final product specifications. |
| | |
| **MAXIMUM RATINGS** | |
| Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability. | |

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