

L-Band Radar Transistor

The high power pulsed radar transistor device part number IB1214M300 is designed for L-Band radar systems operating over the instantaneous bandwidth of 1.215-1.400 GHz. While operating in class C mode this common base device supplies a minimum of 300 watts of peak pulse power under the conditions of 100μs pulse width and 10% duty cycle. All devices are 100% screened for large signal RF parameters.



Silicon Bipolar

- Ultra-high f_T

Class C Operation

- High Efficiency

Common Base Configuration

- Single Power Supply

Gold Metal

- Maximum Reliability

Emitter Ballasting

- Optimum Thermal Distribution

Internal Impedance Matching

- Ease of Use
- Ultra-low Loss Design

Be0 Package

- Unmatched Thermal Reliability

RF Test Fixture

- Broadband
- Matched to 50Ω
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning Allowed

TYPICAL DATA TYPICAL DATA TYPICAL DATA TYPICAL DATA

General Information		Test Sequence	Freq	PIN	RL	POUT	GP	dG	IC	nc	d - IP	Droop	VSWR-S	VSWR-LMT
General Information		Name	(MHz)	(W)	(dB)	(W)	(dB)	(dB)	(A)	(%)	(deg)	(dB)	1.5:1	2:1
IB1214M300		Test Sequence	Freq	PIN	RL	POUT	GP	dG	IC	nc	d - IP	Droop	VSWR-S	VSWR-LMT
		Name	(MHz)	(W)	(dB)	(W)	(dB)	(dB)	(A)	(%)	(deg)	(dB)	1.5:1	2:1
		Min / Max												
Date:	3/4/2009													
Assbly Lot - SN :	508513-17	Nominal	1215	30.8	-15.0	300	9.89		15.000	50.0	--	-0.06	S	P
Wafer :	B4DE-11-3													
Test Fixture :	586	Nominal	1300	34.4	-13.7	300	9.41	1.12	14.190	52.9	--	-0.09	S	P
Pass / Fail :	Device Passes													
OPERATOR:	FB	Nominal	1400	39.9	-14.3	300	8.76		13.510	55.5	-7.0	-0.12	S	P
Phase Mark :	-3													
Pulse:100us-10%	Vcc=40V													

MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Collector-Emitter Voltage	V_{CES}	75	--	V	$V_{BE}=0V$.
BD	Emitter-Base Voltage	V_{EBO}	2	--	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.15	°C/W	$V_{CC}=V1$, $PW=PW1$, $DF=DF1$, $T_F=25\pm5^\circ C$, $P_{out}=300W$
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification.
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C.
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

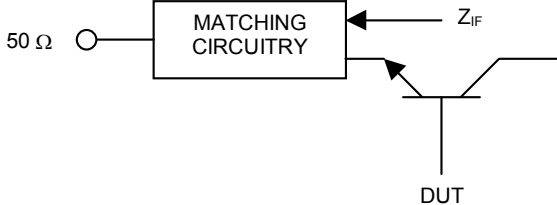
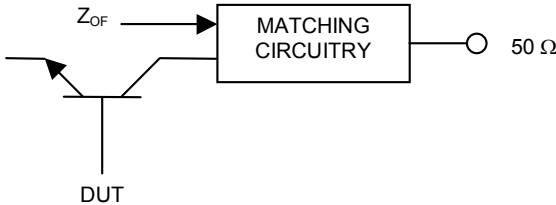
DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Collector-Emitter Breakdown Voltage	BV_{CES}	75	--	V	$I_C=40mA$, $V_{BE}=0V$, $T_F=25\pm5^\circ C$.
100%	Zero Base Voltage Collector Leakage Current	I_{CES}	--	10.0	mA	$V_{CE}=40V$, $V_{BE}=0V$, $T_F=25\pm5^\circ C$.
100%	DC Current Gain	H_{FE}	20	95	--	$V_{CE}=5V$, $I_C=0.5A$, $T_F=25\pm5^\circ C$.

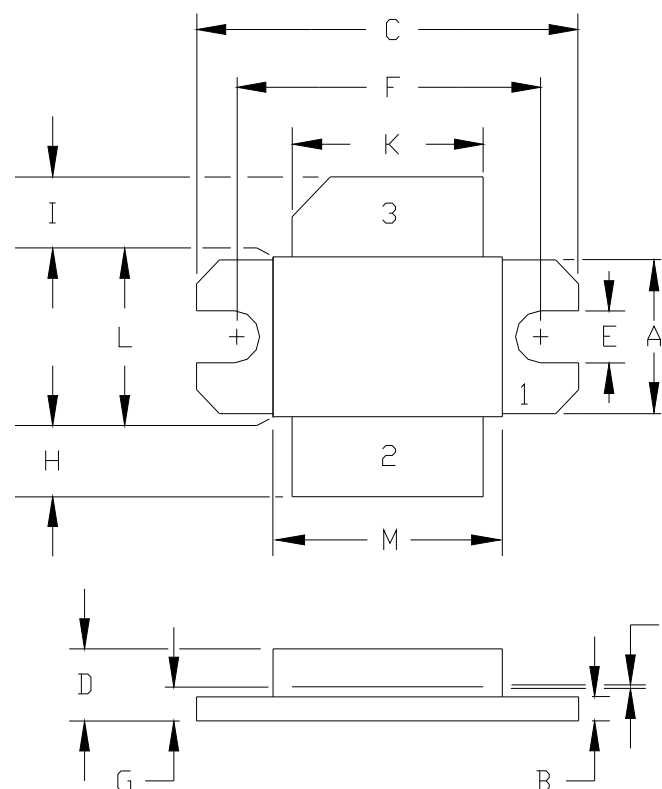
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	RL	-18	-8	dB	$V_{CC}=V1$, $PW=PW1$, $DF=DF1$, $T_F=25\pm5^\circ\text{C}$, $P_{out}=P_{out1}$, P_{out2} , P_{out3} , $F=F1$, $F2$, $F3$.
100%	Input Power	P_{IN}	18.9	60	W	$V_{CC}=V1$, $PW=PW1$, $DF=DF1$, $T_F=25\pm5^\circ\text{C}$, $P_{out}=P_{out1}$, P_{out2} , P_{out3} , $F=F1$, $F2$, $F3$.
100%	Collector Efficiency ($P_O/I_C/V_{CC}$)	N_C	45	75	%	$V_{CC}=V1$, $PW=PW1$, $DF=DF1$, $T_F=25\pm5^\circ\text{C}$, $P_{out}=P_{out1}$, P_{out2} , P_{out3} , $F=F1$, $F2$, $F3$.
100%	Pulse Amplitude Droop	Droop	-0.5	0.5	dB	$V_{CC}=V1$, $PW=PW1$, $DF=DF1$, $T_F=25\pm5^\circ\text{C}$, $P_{out}=P_{out1}$, P_{out2} , P_{out3} , $F=F1$, $F2$, $F3$.
100%	Gain Flatness	dG	--	1.5	dB	Calculate from Gain at each frequency F.
100%	Stability into 1.5:1 VSWR with +0.75dB overdrive	VSWR-S	--	--	--	Repeat P_O with P_{IN} increased by 0.7dB. Rotate 1.5:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristic allowed on detected output pulse.
100%	2:1 Load Mismatch Tolerance	VSWR-LMT	--	--	--	$V_{CC}=V1$, $PW=PW1$, $DF=DF1$, $T_F=25\pm5^\circ\text{C}$, $P_{out}=P_{out1}$, P_{out2} , P_{out3} , $F=F1$, $F2$, $F3$. Rotate 2:1 output VSWR through 360° phase. Post test P_O = Pre test $P_O \pm 10\text{W}$.
100%	Insertion Phase	IP	-20	20	DEG	$V_{CC}=V1$, $PW=PW1$, $DF=DF1$, $T_F=25\pm5^\circ\text{C}$, $P_{out}=P_{out1}$, P_{out2} , P_{out3} , $F=F3$ Measured at middle of Pulse with respect to phase reference, marked in groups of 5 degree margin.
BD	Pulse Risetime	RT	--	80	ns	$V_{CC}=V1$, $PW=PW1$, $DF=DF1$, $T_F=25\pm5^\circ\text{C}$, $P_{out}=P_{out1}$, P_{out2} , P_{out3} , $F=F1$, $F2$, $F3$
Note	$V1 = 40\text{V}$; $PW1=100\mu\text{s}$; $DF1=10\%$; $P_{out1}=$, $P_{out2}=$, $P_{out3}=300\text{W}$; $F1=1.215\text{GHz}$, $F2=1.300\text{GHz}$, $F3=1.400\text{GHz}$.					
Note	T_F = Device flange temperature.					
Note	Screen 'BD' = parameter qualified By Design.					

RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (GHz)	$Z_{IF} (\Omega)$	$Z_{OF} (\Omega)$
1.215	1.17-j2.27	1.42-j1.47
1.300	1.14-j1.77	1.4-j0.81
1.400	1.1-j1.24	1.4-j0.1
Impedance Definition		

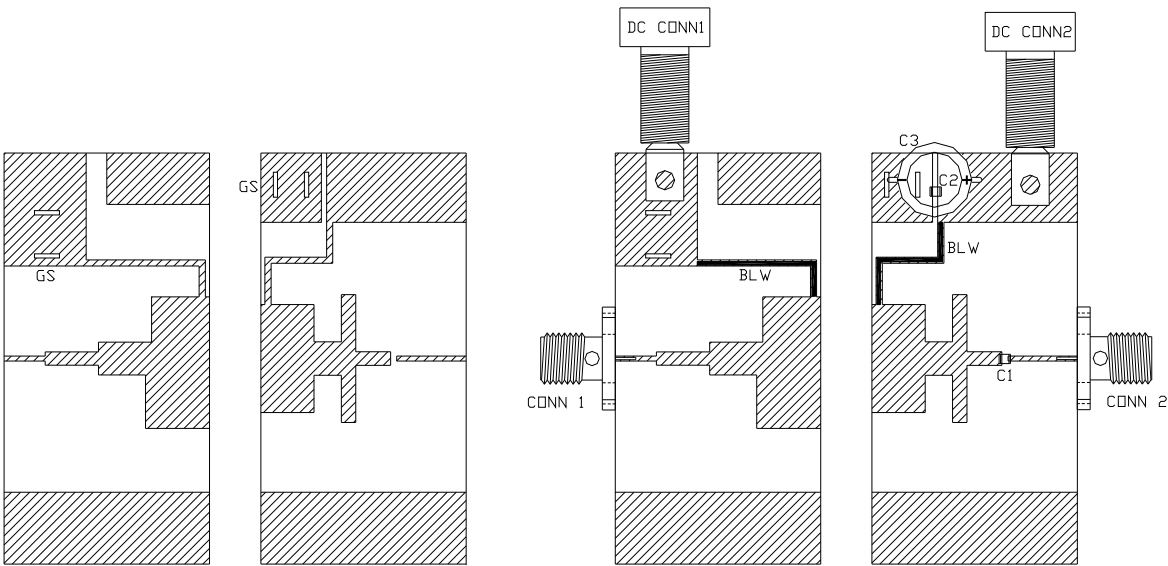
PACKAGE DIMENSIONAL OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.380	0.390	9.65	9.91
B	0.055	0.065	1.40	1.65
C	0.905	1.005	22.99	25.53
D	0.178	0.188	4.52	4.78
E	0.125	0.135	3.18	3.43
F	0.795	0.805	20.19	20.45
G	0.082	0.092	2.08	2.34
H	0.185	0.215	4.70	5.46
I	0.185	0.215	4.70	5.46
J	0.002	0.004	0.05	0.10
K	0.495	0.505	12.57	12.83
L	0.395	0.405	10.03	10.29
M	0.595	0.605	15.11	15.37

PIN SCHEDULE	
1	BASE
2	EMITTER
3	COLLECTOR

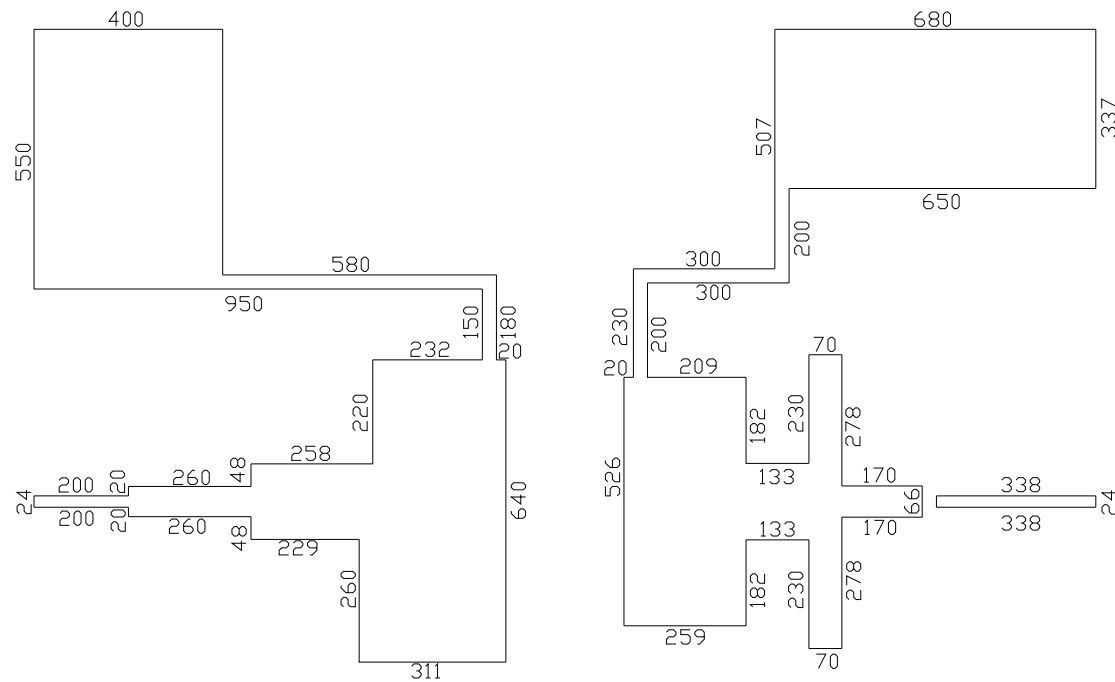
RF TEST FIXTURE



COMPONENT	DESCRIPTION
DUT	TRANSISTOR #IB1214M300, MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS #R03010, TH=0.025" 1oz. Cu
C1, C2	CHIP CAPACITOR, TYPE ATC100A, 100 pF
C3	ELECTROLYTIC CAPACITOR, 68uF / 63V
GS	GROUND SHIM, COPPER, TH=0.001"
CONN1, CONN2	SMA CONNECTOR, TYPE DS #2052-5636-02
INPUT PC BOARD CARRIER	2" INCH BRASS - 03 (1.00")
OUTPUT PC BOARD CARRIER	2" INCH BRASS - 03 (1.00")
TRANSISTOR CARRIER	2" INCH COPPER - 03
TRANSISTOR CLAMP	NDRYL CLAMP - 04
HEATSINK	2" INCH HEATSINK - 11
DC CONN1	BANANA JACK, BLACK
DC CONN2	BANANA JACK, RED
BLW	WIRE 0.022" DIA. TYPICAL
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

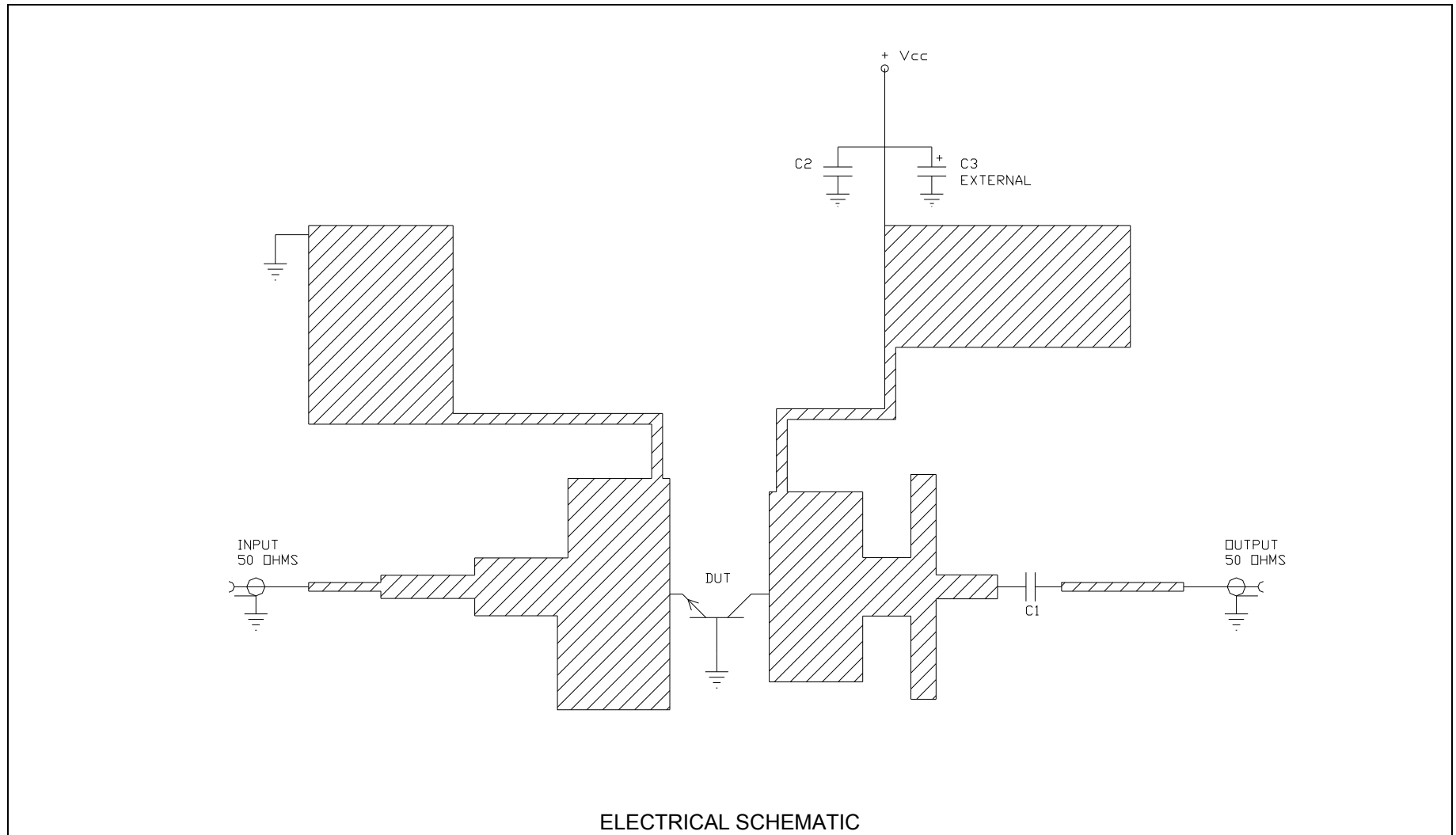
ASSEMBLY AND PARTS LIST

RF TEST FIXTURE



CIRCUIT DIMENSIONS

RF TEST FIXTURE



DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO base is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with general or domestic waste.

DISCLAIMER

Integra Technologies Inc. makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Integra Technologies Inc. assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Integra Technologies Inc. products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Integra Technologies Inc. customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Integra Technologies Inc. for any damages resulting from such improper use or sale.
--