

## L-Band Avionics Transistor

The high power pulsed transistor device part number IB0912M350 is designed for systems operating over the instantaneous bandwidth of 960-1215 MHz. While operating in class C mode under pulsing conditions of 10us/10% and  $V_{cc}=50V$ , this common base device supplies a minimum of 350 watts of peak pulse power. It utilizes a low loss internal input impedance matching structure to yield maximum device gain and to ease the implementation of external matching circuitry. The new generation bipolar transistor geometry utilizes a gold metallization system to achieve maximum reliability. Emitter ballast resistance is incorporated on the active cell for optimum thermal distribution and maximum reliability. All devices are 100% screened for large signal RF parameters.



### Silicon Bipolar

- Ultra-high  $f_T$

### Class C Operation

- High Efficiency

### Common Base Configuration

- Single Power Supply

### Gold Metal

- Maximum Reliability

### Emitter Ballasting

- Optimum Thermal Distribution

### Internal Impedance Matching

- Ease of Use
- Ultra-low Loss Design

### BeO Package

- Unmatched Thermal Reliability

### RF Test Fixture

- Broadband
- Matched to 50Ω
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning Allowed
- Micro-strip structure on soft pc board with dielectric constant 10.2

## TYPICAL DATA TYPICAL DATA TYPICAL DATA TYPICAL DATA

General Information	Test Sequence	Freq	PIN	RL	POUT	GP	dG	IC	nc	Droop	VSWR-S	VSWR-LMT
IB0912M350	Name	(MHz)	(W)	(dB)	(W)	(dB)	(dB)	(A)	(%)	(dB)	1.5:1	3:1
Date:	3/19/2009											
Assbly Lot - SN :	D2559	Nominal	960	33	-18.0	375	10.56		13.290	56.4	0.07	S P
Wafer :	N/A											
Test Fixture :	1348	Nominal	1090	33	-12.0	413	10.97	0.68	14.950	55.3	0.04	S P
Pass / Fail :	Device Passes											
OPERATOR:	FB	Nominal	1215	33	-12.0	353	10.29		12.010	58.8	0.02	S P

**MAXIMUM RATINGS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Collector-Emitter Voltage	$V_{CES}$	--	75	V	--
BD	Emitter-Base Voltage	$V_{EBO}$	--	2	V	--
BD	Storage Temperature Range	$T_{STG}$	-55	+150	°C	--
BD	Operating Junction Temperature Range	$T_J$	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

**THERMAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.090	°C/W	$V_{CC}=50V$ , Pulse format=TACAN, $T_F=25\pm 5^\circ C$ , $P_{IN}=33W$ , $N_C=50\%$
Note	Screen 'BD' = parameter qualified By Design.					

**PROCESSING SPECIFICATIONS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

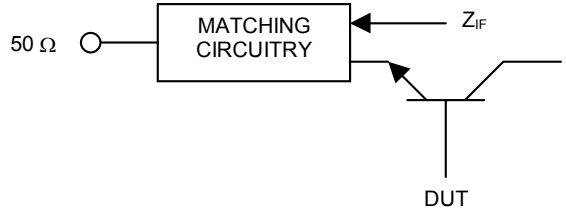
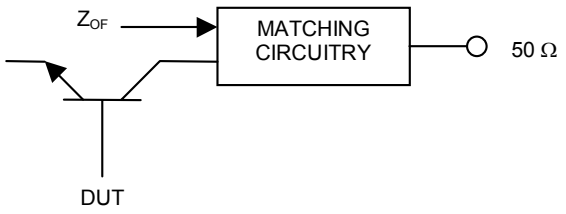
**DC ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Collector-Emitter Breakdown Voltage	$BV_{CES}$	75	--	V	$I_C = 40mA$ , $V_{BE} = 0V$ , $T_F = 25\pm 5^\circ C$ .
100%	Zero Base Voltage Collector Leakage Current	$I_{CES}$	--	100	$\mu A$	$V_{CE} = 50V$ , $V_{BE} = 0V$ , $T_F = 25\pm 5^\circ C$ .
100%	DC Current Gain	$H_{FE}$	20	100	--	$V_{CE} = 5V$ , $I_C = 500mA$ , $T_F = 25\pm 5^\circ C$ .

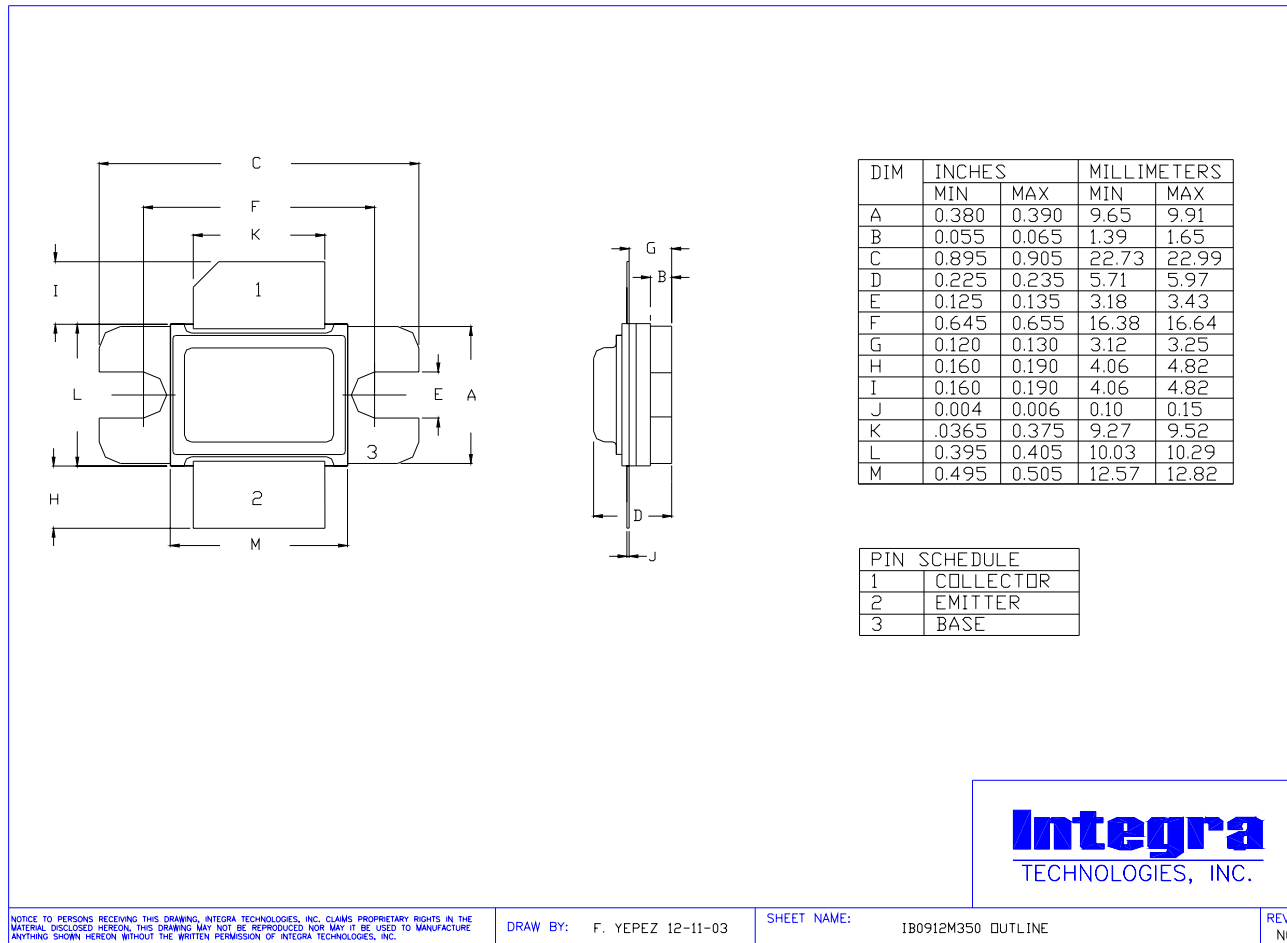
**RF ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	RL	-18	-8	dB	$V_{CC}=50V$ , $P_{IN}=33W$ , Pulse = Note 2, $T_F=25\pm 5^\circ C$ , $F=F1$ .
BD	Maximum Overdrive	$P_{IN(MAX)}$	--	39	W	$V_{CC}=50V$ , Pulse = Note 2, $T_F=25\pm 5^\circ C$ , $F=F1$ .
100%	Power Gain	$G_P$	10.25	11.75	dB	$V_{CC}=50V$ , $P_{IN}=33W$ , Pulse = Note 2, $T_F=25\pm 5^\circ C$ , $F=F1$
100%	Output Power	Pout	350	494	W	$V_{CC}=50V$ , $P_{IN}=33W$ , Pulse = Note 2, $T_F=25\pm 5^\circ C$ , $F=F1$
100%	Collector Efficiency ( $P_o/I_c/V_{CC}$ )	$N_C$	50	75	%	$V_{CC}=50V$ , $P_{IN}=33W$ , Pulse = Note 2, $T_F=25\pm 5^\circ C$ , $F=F1$ .
100%	Pulse Amplitude Droop	Droop	-0.5	0.5	dB	$V_{CC}=50V$ , $P_{IN}=33W$ , Pulse = Note 2, $T_F=25\pm 5^\circ C$ , $F=F1$ .
100%	Gain Flatness	$\Delta G$		1.5	dB	Delta between highest gain and lowest gain from 960-1215MHz
100%	Stability into 1.5:1 VSWR	VSWR-S	--	--	--	$V_{CC}=50V$ , $P_{IN}=33W$ , Pulse = Note 2, $T_F=25\pm 5^\circ C$ , $F=F1$ . Rotate 1.5:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse.
100%	Load Mismatch Tolerance	VSWR-LMT	3:1	--	--	$V_{CC}=50V$ , $P_{IN}=33W$ , Pulse = Note 2, $T_F=25\pm 5^\circ C$ , $F=F1$ . Rotate 3:1 output VSWR through 360° phase. Survival.
Note 1	F1 = 960/1090/1215 MHz.					
Note 2	Pulse width = 10us, Duty Factor = 10%					
Note 3	$T_F$ = Device flange temperature.					
Note 4	Screen 'BD' = parameter qualified By Design.					

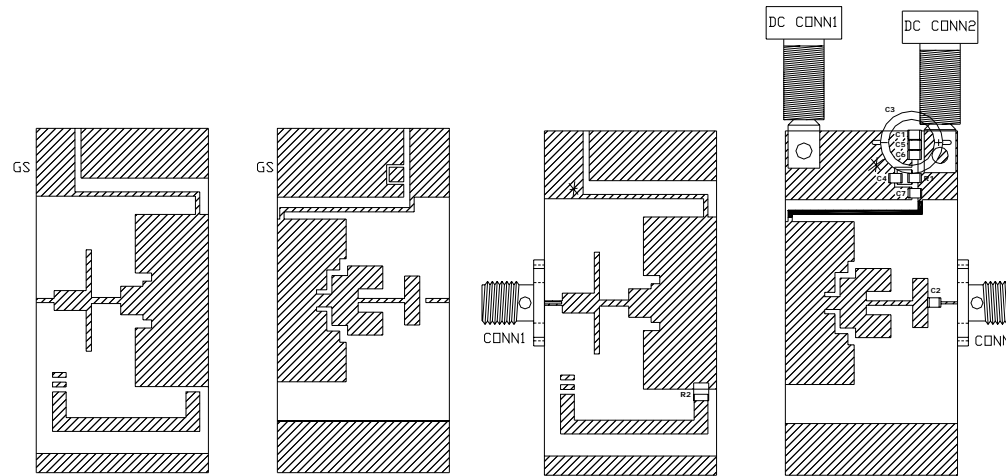
**RF TEST FIXTURE IMPEDANCE CHARACTERISTICS**

Frequency (MHz)	$Z_{IF}$ ( $\Omega$ )	$Z_{OF}$ ( $\Omega$ )
960	1.10-j1.57	1.34-j1.65
1090	1.10-j0.98	1.49-j1.10
1215	1.23-j0.58	1.71-j0.89
Impedance Definition		

**PACKAGE DIMENSIONAL OUTLINE DRAWING**



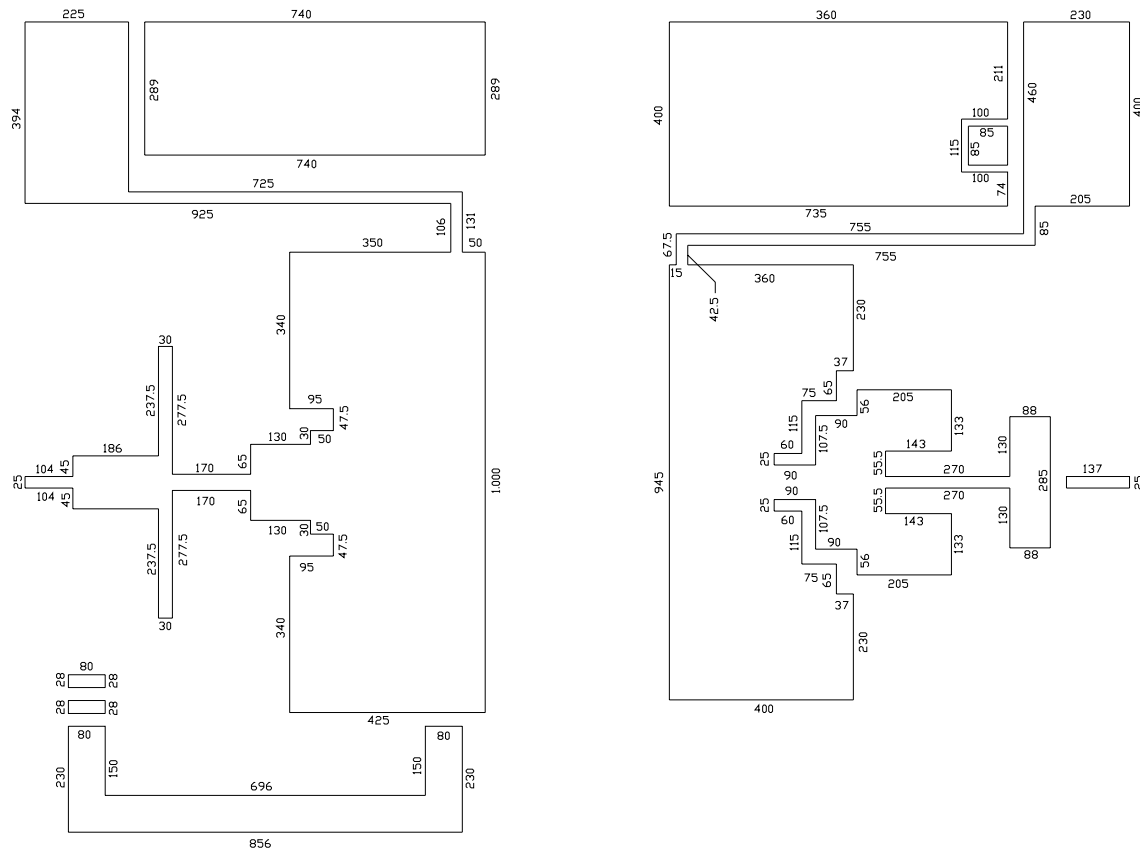
**RF TEST FIXTURE**



COMPONENT	DESCRIPTION
DUT	TRANSISTOR #IB0912M350, MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS #RD6010.2LM .025" 1oz. Cu.
C1, C2	CHIP CAPACITOR, TYPE ATC100A, 100 pF
C3	ELECTROLYTIC CAPACITOR, 68uF / 63V
C4	CHIP CAPACITOR 0.1uF
C5	CAPACITOR 2uF
C6	CAPACITOR 4.7nF 100V K9624 CK05 BX 472K
C7	CHIP CAPACITOR ATC 39pF
C8 (NOT SHOWN)	STORAGE ELECTROLYTIC CAPACITOR 4700uF/50V
R1	CHIP RESISTOR 6.8 OHMS
R2	CHIP RESISTOR 50 OHMS
GS	GROUND SHIM, COPPER, TH=0.001"
CONN1, CONN2	SMA CONNECTOR, TYPE QS #2052-5636-02
INPUT PC BOARD CARRIER	1.00 INCH BRASS - 03
OUTPUT PC BOARD CARRIER	1.00 INCH BRASS - 03
TRANSISTOR CARRIER	2 INCH COPPER - 02
TRANSISTOR CLAMP	NORYL CLAMP -02
HEATSINK	2 INCH HEATSINK - 11
DC CONN1	BANANA JACK, BLACK
DC CONN2	BANANA JACK, RED
BLW	BIAS LINE WIRE - COPPER - 0.022" DIA TYPICAL
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

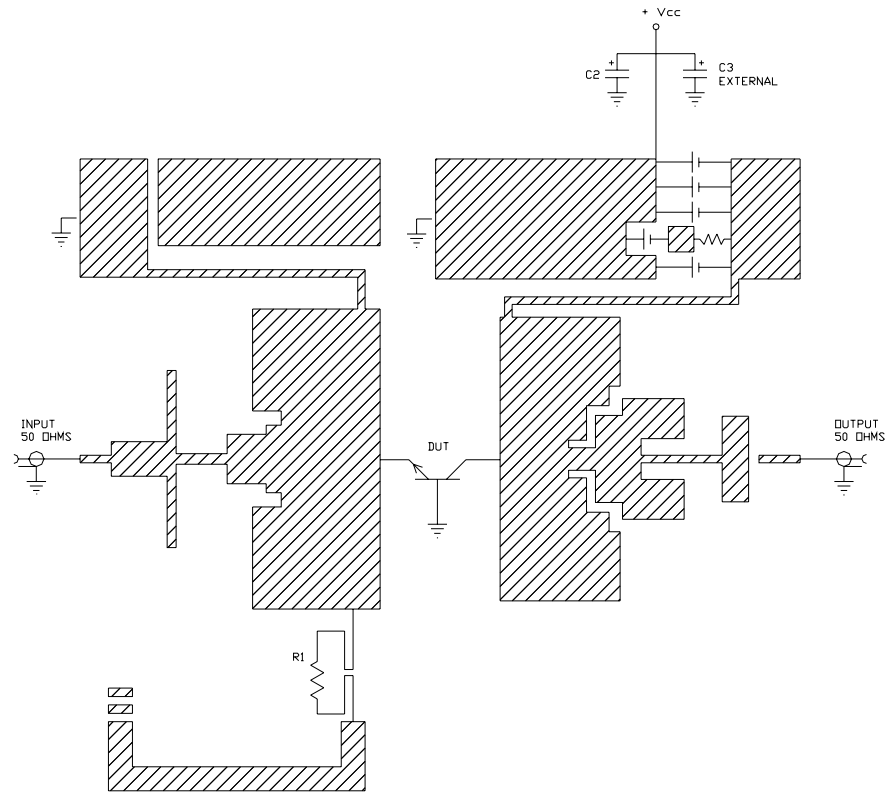
**ASSEMBLY AND PARTS LIST**

**RF TEST FIXTURE**



CIRCUIT DIMENSIONS (mils)

**RF TEST FIXTURE**



**ELECTRICAL SCHEMATIC**

**DEFINITIONS**

<b>Data Sheet Status</b>	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
<b>Maximum Ratings</b>	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only and operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

**WARNING**

<b>Product and environmental safety - toxic materials</b>
This product contains beryllium oxide. The product is entirely safe provided that the BeO base is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with general or domestic waste.

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